This listing of claims will replace all prior versions, and listings of claims in the application:

Amendments To The Claims

1. (Original) A MIS transistor, formed on a semiconductor substrate, comprising:

a semiconductor substrate comprising a projecting part of which the surfaces are at least two different crystal planes on a principal plane;

a gate insulator for covering at least a part of each of said at least two different crystal planes constituting the surface of the projecting part;

a gate electrode comprised by the gate insulator so as to be electrically insulated from the semiconductor substrate, and comprised on each of said at least two different crystal planes constituting the surface of the projecting part; and

a single conductivity type diffusion region formed in the projecting part facing each of said at least two different crystal planes constituting the surface of the projecting part and individually formed on both sides of the gate electrodes.

2. (Original) The MIS transistor according to claim 1 wherein

the channel width of a channel formed along with the gate insulator between the single conductivity diffusion regions individually formed on both sides of the gate electrodes is indicated by summation of the channel widths of each channel generated along said at least two different crystal planes.

3. (Currently Amended) The MIS transistor according to claim 1 or ~~claim 2~~ wherein

the gate insulator covers said at least a part of each of said at least two different crystal planes, which configure the surface of the projecting part, so that said at least two different crystal planes are continuously covered.

4. (Currently Amended) A MIS transistor, according to claim 2 wherein ~~formed on a semiconductor substrate, comprising:~~

~~a semiconductor substrate comprising a projecting part of which the surfaces are at least two different crystal planes on a principal plane;~~

[[a]] the gate insulator ~~for covering~~ covers said at least a part of each of said at least two different crystal planes which ~~constituting the principal plane and~~ configure the surface of the projecting part so that said at least two different crystal planes are continuously covered.

~~a gate electrode comprised by the gate insulator so as to be electrically insulated from the semiconductor substrate, and comprised on each of said at least two different crystal planes constituting the principal plane and the surface of the projecting part; and~~

~~a single conductivity type diffusion region formed in the projecting part facing each of said at least two different crystal planes constituting the principal plane and surface of the projecting part and individually formed on both sides of the gate electrodes.~~

5. (Currently Amended) The MIS transistor formed on a semiconductor substrate, comprising:

a semiconductor substrate comprising a projecting part of which the surfaces are at least two different crystal planes on a principal plane;

a gate insulator for covering at least a part of each of said at least two different crystal planes constituting the principal plane and the surface of the projecting part;

a gate electrode comprised by the gate insulator so as to be electrically insulated from the semiconductor substrate, and comprised on each of said at least two different crystal planes constituting the principal plane and the surface of the projecting part; and

a single conductivity type diffusion region formed in the projecting part facing each of said at least two different crystal planes constituting the principal plane and surface of the projecting part and individually formed on both sides of the gate electrodes.

~~according to claim 4, wherein~~

~~the channel width of the channel generated along the principal plane is complemented with the channel width of the channel generated along a crystal plane, different from the principal plane, of said at least two crystal planes.~~

6. (Currently Amended) The MIS transistor according to ~~claim 4 or~~ claim 5, wherein

the gate insulator covers at least a part of each of said at least two different crystal planes, which configure the principal plane and the surface of the projecting part, so that the principal plane and said at least two different crystal planes are continuously covered.

7. (Currently Amended) The MIS transistor, according to claim 5, wherein

the gate insulator covers at least a part of each of said at least two different crystal planes, which configure the principal plane and the surface of the projecting part, so that the principal plane and said at least two different crystal planes are continuously covered.

~~according to claim 1 or claim 4, being a signal transistor.~~

8. (Currently Amended) The MIS transistor according to claim 6, wherein

the gate insulator covers at least a part of each of said at least two different crystal planes, which configure the principal plane and the surface of the projecting part, so that the principal plane and said at least two different crystal planes are continuously covered.

~~claim 1 or claim 4, wherein~~

~~the semiconductor substrate is a silicon substrate, and~~

~~the gate insulator is formed by exposing the surface of the silicon substrate to a plasma of a prescribed inert gas so as to remove hydrogen, and the hydrogen content at an interface of the silicon substrate and the gate insulator is $10^{11}/cm^2$ or less in units of surface density.~~

9. (Currently Amended) The MIS transistor according to claim 1, being a signal transistor. ~~8, wherein the semiconductor substrate is a silicon substrate, and~~

~~the principal plane and said at least two different crystal planes are any two different crystal planes from the (100) plane, the (110) plane and the (111) plane.~~

10. (Currently Amended) The MIS transistor, according to claim 5, being a signal transistor. ~~A CMOS transistor, comprising the MIS transistor according to claim 1 or claim 4, and also comprising an n-channel MOS transistor only formed on a principal plane of a semiconductor substrate and a p-channel MOS transistor, wherein~~

~~the p-channel MOS transistor comprises~~

~~that the gate insulator is an oxide film, and~~

~~that the single conductivity type diffusion region is a p-type diffusion region.~~

11. (Currently Amended) The MIS transistor according to claim 1, wherein

the semiconductor substrate is a silicon substrate, and

the gate insulator is formed by exposing the surface of the silicon substrate to a plasma of a prescribed inert gas so as to remove hydrogen, and the hydrogen content at an interface of the silicon substrate and the gate insulator is $10^{11}/cm^2$ or less in units of surface density. ~~A CMOS transistor, comprising the MIS transistor according to claim 8, and also comprising an n-channel MOS transistor only formed on a principal plane of a semiconductor substrate and a p-channel MOS transistor, wherein~~

~~the p-channel MOS transistor comprises~~

~~that the gate insulator is an oxide film, and~~

~~that the single conductivity type diffusion region is a p-type diffusion region.~~

12. (Currently Amended) The MIS transistor according to claim 5, wherein

the semiconductor substrate is a silicon substrate, and

the gate insulator is formed by exposing the surface of the silicon substrate to a plasma of a prescribed inert gas so as to remove hydrogen, and the hydrogen content at an interface of the silicon substrate and the gate insulator is $10^{11}/cm^2$ or less in units of surface density.

~~A CMOS transistor comprising the MIS transistor according to claim 1 or claim 4, and also comprising an n-channel MOS transistor and a p-channel MOS transistor on a silicon substrate with the (100) plane as its principal plane, wherein~~

~~the n-channel MOS transistor comprises~~

~~a gate oxide film covering a part of the principal plane alone,~~

~~a gate electrode configured on the principal plane by the gate oxide film so as to be electrically insulated from the silicon substrate, and~~

~~an n-type diffusion region formed in the silicon substrate facing the principal plane and formed on both sides of the gate electrode, and~~

~~the p-channel MOS transistor comprises~~

~~that the single conductivity type diffusion region is a p-type diffusion region;~~

~~that the gate insulator is an gate oxide film, and~~

~~that one crystal plane is the (100) crystal plane and a second crystal plane is the (110) crystal plane among said at least two crystal planes.~~

13. (Currently Amended) The MIS transistor according to claim 11, wherein

the semiconductor substrate is a silicon substrate, and

the principal plane and said at least two different crystal planes are any two different crystal planes from the (100) plane, the (110) plane and the (111) plane. ~~The CMOS transistor according to claim 11, wherein~~

~~the current driving capacity in the p-channel MOS transistor and the n-channel MOS transistor are equal to each other and the element area of the p-channel MOS transistor and the n-channel MOS transistor are the same.~~

14. (New) A CMOS transistor, comprising the MIS transistor according to claim 1, and also comprising an n-channel MOS transistor only formed on a principal plane of a semiconductor substrate and a p-channel MOS transistor, wherein

the p-channel MOS transistor comprises

that the gate insulator is an oxide film, and

that the single conductivity type diffusion region is a p-type diffusion region.

15. (New) A CMOS transistor, comprising the MIS transistor according to claim 5, and also comprising an n-channel MOS transistor only formed on a principal plane of a semiconductor substrate and a p-channel MOS transistor, wherein

the p-channel MOS transistor comprises

that the gate insulator is an oxide film, and

that the single conductivity type diffusion region is a p-type diffusion region.

16. (New) A CMOS transistor, comprising the MIS transistor according to claim 11, and also comprising an n-channel MOS transistor only formed on a principal plane of a semiconductor substrate and a p-channel MOS transistor, wherein

the p-channel MOS transistor comprises

that the gate insulator is an oxide film, and

that the single conductivity type diffusion region is a p-type diffusion region.

17. (New) A CMOS transistor comprising the MIS transistor according to claim 1, and also comprising an n-channel MOS transistor and a p-channel MOS transistor on a silicon substrate with the (100) plane as its principal plane, wherein

the n-channel MOS transistor comprises

a gate oxide film covering a part of the principal plane alone,

a gate electrode configured on the principal plane by the gate oxide film so as to be electrically insulated from the silicon substrate, and

an n-type diffusion region formed in the silicon substrate facing the principal plane and formed on both sides of the gate electrode, and

the p-channel MOS transistor comprises

that the single conductivity type diffusion region is a p-type diffusion region;

that the gate insulator is an gate oxide film, and

that one crystal plane is the (100) crystal plane and a second crystal plane is the (110) crystal plane among said at least two crystal planes.

18. (New) A CMOS transistor comprising the MIS transistor according to claim 5, and also comprising an n-channel MOS transistor and a p-channel MOS transistor on a silicon substrate with the (100) plane as its principal plane, wherein

the n-channel MOS transistor comprises

a gate oxide film covering a part of the principal plane alone,

a gate electrode configured on the principal plane by the gate oxide film so as to be electrically insulated from the silicon substrate, and

an n-type diffusion region formed in the silicon substrate facing the principal plane and formed on both sides of the gate electrode, and

the p-channel MOS transistor comprises

that the single conductivity type diffusion region is a p-type diffusion region;

that the gate insulator is an gate oxide film, and

that one crystal plane is the (100) crystal plane and a second crystal plane is the (110) crystal plane among said at least two crystal planes.

19. (New) The CMOS transistor according to claim 16, wherein the current driving capacity in the p-channel MOS transistor and the n-channel MOS transistor are equal to each other and the element area of the p-channel MOS transistor and the n-channel MOS transistor are the same.